**Internship Plan – Yuzhe Jin**

**Primary Goal:** Integrate a RISC-V processor and NetFPGA into an open source Smart NIC

**Tasks:**

1. NetFPGA
   1. Compile and build a good-known Open-NIC code
   2. Compile the build NetFPGA-plus, fix and broken settings
   3. Run the NetFPGA code, update driver with Open-NIC updates
2. RISC-V
   1. Identify a suitable RISC-V code to use (preference: Alveo compatible)
   2. Compile and build code for Alveo U280
   3. Run the image on the FPGA
3. Integration
   1. Compile NetFPGA and RISC-V on the same device, without integration of interfaces
   2. Compile NetFPGA and RISC-V on the same device, without integration of interfaces
   3. Run the image on the FPGA
4. Development workstation
   1. Install and run Vivado environment on a new workstation

**Weekly Plan:**

Week 1 – Training, get acquainted with previous work and existing code, Tasks 1.a and 1.b

Week 2 – Continue Task 1.b, Task 1c

Weeks 3 – Task 2, Task 4 (estimated)

Week 4- Finish Task 2, start task 3.a

Weeks 5,6 – Task 3